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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,975	12/05/2003	Takeshi Irie	33035M136	7221

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EXAMINER	
LIVEDALEN, BRIAN J	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/727,975	IRIE, TAKESHI	
	Examiner	Art Unit	
	Brian J. Livedalen	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/5/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama et al. (US 6188059) in view of Nishiyama et al. (US 6333804) hereinafter referred to as Nishiyama'804.

In regard to claims 1, 5, and 6 Nishiyama discloses (fig. 2) an avalanche photo diode (1) for receiving signal light and generating a photo current corresponding to the signal light; a first current mirror (2F) having a pair of current path (column 1 line 48); the photo diode being connected to one of the current path and a high voltage source (Vapd) for supplying a bias potential to the photo diode, wherein the pair of the current path of the first current mirror circuit is connected to the high voltage source and the avalanche photo diode is biased by the high voltage source through the first current mirror circuit; a second current mirror circuit (2R) having a pair of current path, a first terminal, a second terminal, a third terminal and a fourth terminal, the first terminal and

second terminals being connected to one of the paired current path at each ends thereof, the third and fourth terminals being connected to the other of the paired current path at each ends thereof, the first terminal being connected to the other of the paired current path of the first current mirror circuit; a signal detection circuit connected to the second terminal of the second current mirror circuit (column 8, lines 14 and 15); a current monitor terminal (IMT) connected to the third terminal of the second current mirror circuit. Nishiyama remains silent regarding a voltage source connected to the third terminal of the second current mirror circuit for supplying a bias to the other of the paired current path of the second current mirror circuit. However, Nishiyama'804 discloses (fig. 7) an optical receiver employing two current mirror circuits and a voltage source (Vcc) attached to the third terminal of the second mirror circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the voltage source of Nishiyama'804 to the optical receiver of Nishiyama so that the current monitor can be changed while the ratio between the respective currents flowing through both transistors of the current mirror circuit are held constant.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama et al. (US 6188059) in view of Nishiyama et al. (US 6333804) as applied to claim 1 above, and further in view of Bodig et al. (5075627).

In regard to claims 2 and 3, Nishiyama in view of Nishiyama'804 disclose (fig. 2) an optical receiver having two current mirror circuits and a voltage supply connected to the second current mirror circuit. Nishiyama in view of Nishiyama'804 remains silent regarding the nature of the voltage source. However, Bodig discloses (fig. 1) a voltage

source having two resistors (R7 and R8) in series acting as a voltage divider; the first resistor being connected to the power supply (5V) and a diode (D5); the second resistor being connected to the diode and a ground. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the voltage supply of Bodig to the optical receiver of Nishiyama in view of Nishiyama'804 in order to control the direction of current and limit the voltage source.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama et al. (US 6188059) in view of Nishiyama et al. (US 6333804) as applied to claim 1 above, and further in view of Yuasa (6034518).

In regard to claim 4, Nishiyama in view of Nishiyama'804 disclose (fig. 2) an optical receiver having two current mirror circuits and a voltage supply connected to the second current mirror circuit. Nishiyama in view of Nishiyama'804 remain silent regarding the bias voltage of the voltage source. However Yuasa discloses biasing a voltage source less than 2.5 volts and greater than 1.5 volts when used to stabilize current (column 7, lines 9-13). It would have been obvious to one of ordinary skill at the time the invention was made to include the voltage limitations of Yuasa in order to effectively stabilize the current mirror circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Livedalen whose telephone number is (571) 272-2715. The examiner can normally be reached on 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bjl

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